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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,996	09/19/2005	Joji Fujiwara	MAT-8744US	1009

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EXAMINER	
CRAWFORD, LATANYA N	
ART UNIT	PAPER NUMBER
2809	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,996	FUJIWARA ET AL.	
	Examiner	Art Unit	
	LaTanya Crawford	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/19/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/19/2005*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1,15, & 17** are rejected under 35 U.S.C. 102*(e)* as being anticipated by **Aoyagi (US Patent 6,884,938 B2).**

Regarding Claim 1, Aoyagi et al. discloses a circuit module comprising: a substrate **1(column 3, lines 14-16)**; a partition **5** formed on the substrate **1,** the partition **5** having a predetermined height to divide the substrate into a plurality of circuit blocks **4 (fig.1; column 3, line 20-22)**; a sealing member **10** covering the plurality of circuit blocks **(column 3, lines 56-58)**; and a conductive film covering at least a surface of the sealing member **10,** wherein the plurality of circuit blocks are electrically shielded individually **(column 4, lines 4-7)**.

Regarding Claim 15, Aoyagi et al. discloses the partition 5 is higher than an electric component mounted **9** on the substrate **2 (view fig. 1., (column3, lines 45-46))**.

Regarding claim 17, Aoyagi et al. discloses a method for manufacturing a module component having a plurality of circuit blocks shielded individually, the method

comprising: a first step of mounting a partition **5** higher than the mounting components **9**, the partition dividing mounting components and a substrate into a plurality of circuit blocks **4** on the substrate **1(fig.1; column 3, line 14-23)**; a second step of forming a sealing member **10** covering the plurality of circuit blocks individually in such a manner as to be higher than the mounting components **(fig. 1; column 3, line 56-58)**; and a third step of forming a conductive film on a surface of the sealing member **10 (column 4 , lines 5-7)**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,3,5, 8, 9, 10, 13, 14, 16, & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Tsuneoka (US 2004/0252475 A1).**

Regarding Claim 2, Aoyagi et al. invention discloses all of the claimed limitations of claim 1, and further teaches the substrate **1** is made of resin **(column 4, lines 58-61)** but fails to teach the partition is made of resin and conductive material; and the sealing member and the partition contain a same resin.

However, Tsuneoka et al. teaches the partition **70 (view fig. 5; [0025], lines 1-3; [0026] lines 1-3)** is made of resin and conductive material **(view fig. 5; [0028], lines 1-9)**; and the sealing member **40** and the partition **70** contain a same resin **(view fig. 5; [0028], lines 1-9).**

4. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with partition and sealing member containing the same resin taught by Tsuneoka et al. Doing so would provide good heat resistance and good thermal conductivity.

Regarding Claim 3, Aoyagi et al. invention discloses all of the claimed limitations of claim 1, and further teaches the substrate is ceramic (column 4, lines 58-61), but fails to teach the partition is made of ceramic powder-containing resin and conductive material; and the sealing member and the partition contain a same resin.

However, Tsuneoka et al. teaches the partition **70 (view fig. 5; [0025], lines 1-3; [0026] lines 1-3)** is made of ceramic powder-containing resin and conductive material **20 (view fig. 5; [0028], lines 1-9)**; and the sealing member **40** and the partition **70** contain a same resin **(view fig. 5; [0028], lines 1-9).**

5. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with partition and sealing member containing the same resin taught by Tsuneoka. Doing so would provide good heat resistance and good thermal conductivity.

Regarding Claim 5, Aoyagi et al. teaches the conductive material of the partition is a conductive resin **(column 3, lines 33-37).**

Regarding claim 8, Aoyagi et al. invention discloses all of the claimed limitations of claim 1 but fails to teach the partition has a conductive wall in a direction vertical to the substrate.

However, Tsuneoka et al. teaches the partition **70** has a conductive wall **20** in a direction vertical to the substrate **10 (view fig. 5)**.

6. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with the partition or sealing body having a vertical metal film to the substrate taught by Tsuneoka. Doing so would provide good shielding properties.

Regarding claim 9, Aoyagi et al. invention discloses all of the claimed limitations from above but fails to teach the partition is formed by stacking at least one metal film and resin, and the metal film is formed to be parallel with the longitudinal direction of the partition and to be vertical to the substrate.

However, Tsuneoka et al. teaches the partition is formed by stacking at least one metal film **20** and resin **70**, and the metal film is formed to be parallel with the longitudinal direction of the partition and to be vertical to the substrate **(fig 5)**.

7. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with stacking atleast one metal film and resin taught by Tsuneoka et al. Doing so provides good shielding properties.

Regarding claim 10, Aoyagi et al. invention discloses all of the claimed limitations from above but fails to teach the partition has resin at least one side surface thereof.

However, Tsuneoka et al. teaches the partition **70** has resin at least one side surface thereof **(view fig. 5)**.

8. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with the partition or sealing body with a resin on atleast one side taught by Tsuneoka et al. Doing so would provide a low-resistance electrical connection between the partition and housing of an electrical device.

Regarding claim 13, Aoyagi et al. invention discloses all of the claimed limitations from above but fails to teach the partition has a planar shape of a letter T.

However, Tsuneoka et al. teaches the partition **70** has a planar shape of a letter T **(fig. 4)**.

9. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with the partition or sealing body having a planar shape of a letter T. Doing so would provide predetermined circuit blocks to divide mount devices.

Regarding claim 14, Aoyagi et al. invention discloses all of the claimed limitations form above but fails to teach the conductive film is one of metal and conductive resin.

However, Tsuneoka et al. teaches the conductive film **20** is one of metal and conductive resin **([0023] lines 1-2).**

10. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with a conductive metal film taught by Tsuneoka et al. Doing so would provide sufficient shield effect.

Regarding claim 16, Aoyagi et al. invention discloses all of the claimed limitations form above but fails to teach the substrate has a ground pattern on a surface thereof, and the ground pattern is connected with the conductive film.

However, Tsuneoka et al. teaches the substrate **10** has a ground pattern **50** on a surface thereof, and the ground pattern **50** is connected with the conductive film **20 ([0018] lines 15-17).**

11. Given the teachings of Tsuneoka et al. it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with the substrate having a ground pattern connected with the conductive film taught by Tsuneoka et al. Doing so would provide enhanced shield effects.

Regarding claim 20, Aoyagi et al. invention discloses all of the claimed limitations from above but fails the third step includes a step of connecting the conductive film with a ground pattern.

However, Tsuneoka et al. teaches connecting the conductive film **20** with a ground pattern **50 ([0018], lines 15-17)**

12. Given the teachings of Tsuneoka et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the circuit module of Aoyagi et al. with connecting the conductive film with a ground pattern taught by Tsuneoka et al. Doing so would provide a reliable shield effect.

Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Tsuneoka (US 2004/0252475 A1)** applied to claim(s) above and further in view of **Warren (US 2002/0126018 A1).**

Regarding claim 4, Aoyagi et al. as modified by Tsuneoka et al., discloses all of the claimed limitations from above but fails to teach the partition is a metal foil.

However, Warren et al. teaches the partition **210** is a metal foil **([0032] lines 1-3).**

13. Given the teachings of Warren et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with a shielding partition constructed of metal foil taught by Warren et al. Doing so would provide improved performance and reduction of coupling between electronic components.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Warren (US 2002/0126018 A1)** and further in view **Oda (US 2002/0051340).**

Regarding Claim 6, Aoyagi et al. invention as modified by Warren et al., discloses all of the claimed limitations from above but fails to teach the partition is resin

having a metal film formed on an outer surface thereof, and has a square cross section in a longitudinal direction.

However Tsuneoka et al. teaches the partition **70** is resin having a metal film **20** formed on an outer surface thereof **(fig. 5).** Oda et al. further teaches the partition **94A** having a square cross-section in a longitudinal direction **(fig 9; [0048], lines 1-2).**

14. Given the teachings of Oda et al, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al. with a partition having a square cross section taught by Oda et al. Doing so would provide improved efficiency of the module.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Oda (US 2002/0051340)** as applied to claim(s) above and further in view of **Witty (US 6,380,491 B1).**

Regarding claim 7, Aoyagi et al. invention as modified by Oda et al., discloses all the claim language from above but fails to teach the partition is resin having a metal film formed on an outer surface thereof, and has a cross section with a protruding base in a longitudinal direction.

However, Tsuneoka et al. teaches the partition **70** is resin having a metal film **20** formed on an outer surface thereof **(fig. 5).** Witty et al. further teaches a partition **102** having a cross section with a protruding base in a longitudinal direction **(column 3, lines 1-3).**

15. Given the teachings of Witty et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit module of Aoyagi et al.

with a partition having a protruding base taught by Witty et al. Doing so would provide improved shield efficiency.

Claim 11 &12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Witty (US Patent 6,380,491 B1)** as applied to claim(s) above, and further in view of **Learmonth (US Patent 6,049,468).**

Regarding claim 11, Aoyagi et al. invention as modified by Witty et al. discloses all the claim language from above but fails to teach the partition is positioned inside the substrate, and has a planar shape of one of a circle and a polygon.

However, Learmonth et al. discloses the partition **50** is positioned inside the substrate **14**, and has a planar shape of one of a circle and a polygon **(fig. 4)**.

16. Given the teachings of Learmonth et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the circuit module of Aoyagi et al. with a partition position inside the substrate having a planar shape of a polygon taught by Learmonth et al. Doing so would permit the partition to act as a spacer to maintain constant thickness of a PC card and thereby resist flexing of the PC card without damage to the circuit board.

Regarding claim 12, Aoyagi et al. invention as modified by Witty et al. discloses all the claim language from above but fails to teach the partition is positioned out of contact with an outer edge of the substrate.

However, Learmonth et al. discloses the partition **50** is positioned out of contact with an outer edge of the substrate **14 (fig. 4).**

17. Given the teachings of Learmonth et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the circuit module of Aoyagi et al. with a partition position inside the substrate having a planar shape of a polygon taught by Learmonth et al. Doing so would permit the partition to act as a spacer to maintain constant thickness of a PC card and thereby resist flexing of the PC card without damage to the circuit board.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Learmonth (US Patent 6,049,468)** applied to claim(s) above, and further in view of **Napolitano (US 2002/0111015 A1).**

Regarding claim 18, Aoyagi et al. invention as modified by Learmonth et al. discloses all of the claimed limitations from above. Aoyagi et al. further teaches the partition contains a conductive material formed in a direction vertical to the substrate **(fig. 1; column 3 (lines 32-36)** and a sealing member **10** but fails to teach the second step includes a step of polishing the sealing member so as to expose the conductive material on a surface.

However, Napolitano et al. teaches a step of polishing a dielectric layer **21**, so as to expose the conductive material **20** and **15** on a surface **([0022], lines 8-10).**

18. Given the teachings of Napolitano et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the circuit module of Aoyagi et al. with polishing an insulating material or resin to expose the conductive material taught by Napolitano et al. Doing so provides exposure to the interconnection elements.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Aoyagi (US Patent 6, 884,938 B2)** in view of **Napolitano (US 2002/0111015 A1)** as applied to claim(s) above and further in view of **Percival (US Patent 4,691,434).**

Regarding claim 19, Aoyagi et al. invention as modified by Napolitano et al., discloses all of the claimed limitations from above but fails to teach a step of removing the conductive material by one of dicing and laser.

However, Percival et al. teaches a step of removing the conductive material by one of dicing and laser **(Abstract, lines 8-14).**

19. Given the teachings of Percival et al., it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the circuit module of Aoyagi et al. with removing the conductive material by laser taught by Percival et al. Doing so provides connections to underlying electronic components.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited for disclosing related limitations of the applicant's claimed and disclosed invention: **Barnes et al. & Tsuneoka et al. (452').**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Crawford whose telephone number is (571) 270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM -5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Terrell McKinnon can be reached on (571) 272-4797. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Crawford

May 22, 2007

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